In re Patent Application of:
JAYNES ET AL.
Serial No. **10/653,317**
Filed: **SEPTEMBER 2, 2003**
_____/

In the Specification:

Please replace the paragraph bridging pages 8 and 9, with the following rewritten paragraph:

As a non-limiting example, such a predictable bit pattern may correspond to the consecutive frame synchronization patterns or octets that occur in SONET data, referenced above. In order to take advantage of such data for compensator training purposes, frame synchronization octets may initially be detected in the received data stream (or some derivative thereof) and then time-aligned or synchronized with undistorted versions of the synchronization bit patterns. Synchronized distorted and undistorted versions of signals based on the detected synchronization bit patterns may then be applied to the coefficient update unit 40 and to the error generator 70 (through the signal selector 80), respectively, at process-determined times to update IIR filter coefficients. This process of known pattern detection and synchronization for the purpose of compensator or equalizer training may be of the type described in our co-pending U.S. Patent Application Serial [[10/***,***]]10/462,559, filed on June 16, 2003, entitled: "Updating Adaptive Equalizer Coefficients Using Known or Predictable Bit Patterns Distributed Among Unknown Data" (hereinafter referred to as the [['***]]'559 application, assigned to the assignee of the present application and the disclosure of which is incorporated herein.

Please replace the paragraph bridging pages 9 and 10, with the following rewritten paragraph:

Relative to the present invention, training signals with associated control ("gating") signals are generated by an external process or operator (which may correspond to that described in the [['***]]'559 application) and are coupled to the error generator 70 through the signal selector 80 and to the coefficient update unit 40. Signals containing channel-distorted patterns useful for compensator training are coupled from path A to input port 41 of the coefficient update unit 40. Signals containing corresponding undistorted versions of the patterns are coupled over path D to input port 82 of the signal selector 80. A coefficient update control signal that is synchronized with the occurrence of detected training patterns is coupled over path F to input port 44 of the coefficient update unit 40. It is important to note that different levels of delay (not shown in Figure) may be required along respective signal paths A, B, and C, in order to achieve proper compensator operation. These delays may actually be incorporated in selected compensator components, such as the coefficient update unit 40, error generator 70, and the signal switch 80.